Trapping phenomena in AlGaN and InAlN barrier HEMTs with different geometries

Abstract

Trapping effects were evaluated by means of pulsed measurements under different quiescent biases for GaN/AlGaN/GaN and GaN/InAlN/GaN. It was found that devices with an AlGaN barrier underwent an increase in the on-resistance, and a drain current and transconductance reduction without measurable threshold voltage change, suggesting the location of the traps in the gate-drain access region. In contrast, devices with an InAlN barrier showed a transconductance and a decrease in drain associated with a significant positive shift of threshold voltage, indicating that the traps were likely located under the gate region; as well as an on-resistance degradation probably associated with the presence of surface traps in the gate-drain access region. Furthermore, measurements of drain current transients at different ambient temperatures revealed that the activation energy of electron traps was 0.43 eV and 0.38 eV for AlGaN and InAlN barrier devices, respectively. Experimental and simulation results demonstrated the influence of device geometry on the observed trapping effects, since devices with larger gate lengths and gate-to-drain distance values exhibited less noticeable charge trapping effects.

Keywords: GaN-based HEMTs, gate length, gate-to-drain distance, pulsed measurements, trapping effects, virtual gate, drain current transient

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have been demonstrated to be promising candidates for commercial RF power and high-voltage switching applications, especially at high temperature [1–4]. This suitability is due to the physical properties of GaN, such as wide bandgap, high breakdown voltage, and high electron mobility and saturation velocity. The intensive research carried out by many groups worldwide has led to the optimization of different aspects of HEMTs, among which are material quality and control of the surface [5]. Consequently, record device performances have been achieved in recent years. Nakajima *et al* reported a high output power of 900 W at 2.9 GHz and 81 W at 9.5 GHz [6], whereas Chung *et al* presented a cut-off frequency (f_T) of 224 GHz [7] and a maximum frequency (f_{max}) of 300 GHz [8]. Recently, 150 nm gate length T-gate devices, grown on Si substrates, have reached a Johnson's figure of merit of 8.32 THz V [9]. Moreover, great efforts have been made in the investigation of lattice-matched InAlN-barrier HEMTs since they could potentially present no strain, which could improve the heterostructure stability [10] and long term reliability. A higher 2-dimensional electron gas (2DEG) density would be induced mainly by the larger spontaneous polarization compared to the AlGaN barrier [10–12]. Jardel *et al* presented devices with excellent power performance even in Ku band [13], and Lee *et al* reported lattice-matched InAlN/GaN HEMTs with an InGaN back barrier on a SiC substrate showing a record f_T of 300 GHz for 30 nm gate length devices [14].

In spite of the excellent results shown in recent years, GaN-based device performance can still be limited by

dispersion effects related to the presence of surface, bulk, or interface traps [15–17]. One of the most well-known trapping phenomena is the current collapse, which is a temporary recoverable reduction in drain current (I_D) under the application of a high drain field in the ON-state [17, 18]. The performance degradation due to charge trapping is related to intrinsic and extrinsic degradation mechanisms. Whereas the intrinsic effects are present prior to device operation, the extrinsic effects are generated by stressing the device during operation. The intrinsic effects are related to defect states which appear during growth and fabrication. They range from point defects (impurities and vacancies) to structural defects (threading dislocations, stacking faults, or screw dislocations) [19].

The evaluation of trapping effects is essential because they are not only a performance-limiting factor, but also a key issue in terms of reliability [18]. There are several techniques for the characterization of trapping phenomena in GaN-based HEMTs, as described in [17]. For example, gate (drain) lag measurements, based on the analysis of the I_D delay in response to a gate (drain) voltage change, can provide information on the time constants of the trapping phenomena [16, 20]. Double-pulse I_D–V_{DS} and I_D–V_{GS} measurements allow the quick and reliable characterization of current collapse, as well as the extraction of valuable information regarding changes in I_D, threshold voltage (V_{TH}), and on-resistance (R_{ON}) [17, 21]. The study of I_D transients from OFF-state (a negative gate bias lower than V_{TH}, or a high drain-gate voltage) to ON-state through multi-exponential transient measurements provides accurate extraction of the trap activation energy (E_A) applying the Arrhenius plot [20, 22].

On the other hand, the optimal device layout design depends on the specific application requirements. In general, sub-micron gate length (L_G) devices are more suitable for RF applications, whereas larger gate-to-drain distance (L_{GD}) increases the breakdown voltage (V_{BD}). However, other factors, such as the influence of the geometry on self-heating, need to be considered during the device design [23]. Similarly, the device geometry may also affect the trapping effects observed; however, no results concerning this topic have been found in the literature. Therefore, a deep study, by means of both, experimental and simulation tools, can be useful for the optimization of the device design.

In this paper, we present an extensive analysis of trapping phenomena in both GaN/AlGaN/GaN and GaN/InAlN/GaN HEMTs, and quantify the possible location and E_A of measured trap levels. Moreover, we evaluate the trapping effects as a function of the device geometry (mainly L_G and L_{GD}) to demonstrate its influence on the DC-RF dispersion.

2. Experimental details

The heterostructures were grown by metal-organic chemical vapour deposition (MOCVD) on 4H-SiC substrates. The detailed structure of the samples is the following: 1 nm GaN/22 nm $Al_{0.29}Ga_{0.71}N$/1.4 μm GaN/400 μm 4H-SiC; and 3 nm GaN/10 nm $In_{0.17}Al_{0.83}N$/1 nm AlN/2 μm GaN/300 μm 4H-SiC. An inductive coupled plasma (ICP) etch (Cl_2/Ar, 5 mTorr, 150/40 W ICP/RIE power, 160 V dc bias, approximately 100 nm step) was performed for electrical device isolation. Ohmic contacts were formed by e-beam evaporation of Ti/Al/Ni/Au (20/120/40/80 nm) annealed at 850 °C for 30 s in N_2 atmosphere. The gate electrode was created evaporating a Ni/Au (20/200 nm) bilayer, with a one-finger layout. Then, a Si_xN_y passivation layer of 100 nm thick was deposited by plasma enhanced chemical vapour deposition (PECVD). Figure 1 shows a picture and a simplified scheme of the devices under study.

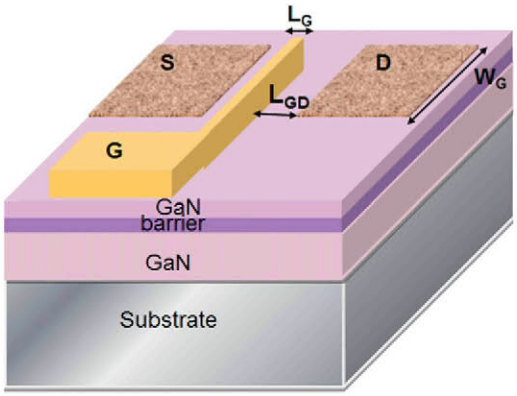

Figure 1. Simplified scheme of one-finger devices.

Preliminary dc characterization was performed in devices with $W_G = 100\,\mu$m, $L_G = 3\,\mu$m, and $L_{GD} = 10\,\mu$m. Table 1 shows the main electrical parameters obtained. The on-resistance (R_{ON}) was calculated as the inverse of the slope of the linear fitting of drain current (I_D) in the linear region for $V_{GS} = 0$ V. The threshold voltage (V_{TH}) was extracted from the intercept of the fitting line of the transconductance (g_m), whereas the carrier concentration (n_s) and the mobility (μ_H) were extracted from the Hall measurements done in Van der Pauw structures. InAlN barrier devices showed better dc performance, as evidenced by a higher $I_{D.max}$ and $g_{m.max}$ as well as lower R_{ON}.

The equipment used in the pulsed measurements consisted of a low/high temperature Janis probe station and a system formed by a Yokogawa DLM2000 digital oscilloscope and an Agilent 81150A pulse function arbitrary noise generator, remotely controlled by software. Figure 2 shows the scheme of the set-up.

Trapping effects were evaluated by double-pulsed measurements similarly to those described in the literature [17, 21]. In these measurements, the device was first biased in OFF-state during 99 μs (τ_{OFF}), and then turned to the ON-state by changing the gate and drain voltages synchronously during a pulse width (τ_{ON}) of 1 μs. As table 2 reports, five different quiescent points (Q points) were adopted. Point A was taken as reference since it presents negligible electron trapping. In the case of the other Q points, increasing the $V_{DS.Q}$ the gate-to-drain reverse bias is also increased, which leads to more trapping effects.

Table 1. Typical electrical parameters measured in the studied devices.

DEVICES	$I_{D.max}$ (A mm^{-1})	R_{ON} (Ω mm^{-1})	$g_{m.max}$ (mS mm^{-1})	V_{TH} (V)	$n_{s.max}$ (10^{+12} cm^{-2})	μ_H (cm^2 V^{-1} s^{-1})
AlGaN	0.51	7.5	170.0	−4.2	9.5	1560
InAlN	0.91	6.7	177.6	−7.6	19	1509

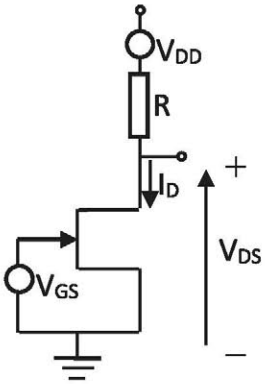

Figure 2. Scheme of the set-up.

Table 2. Description of the Q points used to evaluate the trapping effects.

	Q POINT				
	A	B	C	D	E
$V_{GS.Q}$	0 V	$<V_{TH}$	$<V_{TH}$	$<V_{TH}$	$<V_{TH}$
$V_{DS.Q}$	0 V	0 V	10 V	15 V	20 V

Afterwards, measurements of I_D transients were performed to characterize the traps. Devices were kept in different trapping biases ($V_{GS.F}$, $V_{DS.F}$) for 100 s, and then switched to an ON-state bias ($V_{GS.M}$, $V_{DS.M}$), recording I_D from 1 μs to 200 s. Bisi *et al* demonstrated that the choice of the bias ($V_{GS.M}$, $V_{DS.M}$) used for the measurement of the transient I_D can strongly affect the results [21]. Moreover, they also concluded that the use of proper trap filling voltages could provide valuable information about the location of the traps [21]. Therefore, devices were tested at 80 °C using two different biases ($V_{GS.M}$, $V_{DS.M}$), one in the linear region (M1), and the other in the saturation region (M2) to choose the optimal bias point. In addition, three different trap filling voltages ($V_{GS.F}$, $V_{DS.F}$) were also used, two in OFF-state (F1 and F2) and one in semi ON-state (F3), in order to select the more adequate trap filling voltages. I_D transient measurements at different ambient temperatures (T_{amb}) were carried out and the activation energy of the traps (E_A) was extracted from the Arrhenius plot. The following stretched multi-exponential function was used to fit the I_D transients:

$$I_D(t) = I_{D.final} - \sum_i^N A_i \cdot e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \quad (1)$$

where A_i is the amplitude, τ_i the typical time constant and β_i is the non-exponential stretching-factor of the N detected charge emission ($A_i > 0$) or capture ($A_i < 0$) processes. Depending on the sample under study, N can take values in between 2 and 4 [21]. We used this function due to its good accuracy reported in [21] in comparison with other fitting methods [18, 24].

Finally, we evaluate the influence of device geometry (L_G and L_{GD}) on the observed trapping effects. To do so, V_{GS}-pulsed measurements defined as gate turn-on measurements in [20] were carried out using a fixed period (τ) of 4 ms and variable pulse width (τ_{ON}) from 1 ms to 1 μs in devices with different geometries.

3. Results and discussion

3.1. Trapping phenomena analysis

Double pulsed measurements in dark revealed a reduction of the device performance possibly caused by the presence of traps. As figure 3(a) illustrates, devices with AlGaN barrier presented a reduction of I_D and an increase in R_{ON}, which are approximately of 20% and 30%, respectively, for the

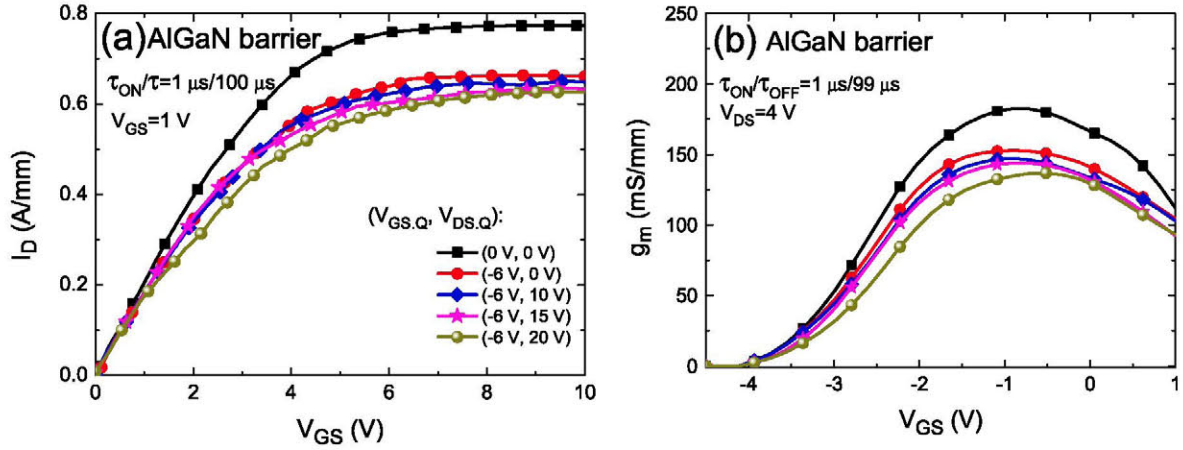

Figure 3. (a) I_D and (b) g_m (derived from I_D–V_{GS}) pulsed characterization for an AlGaN barrier device.

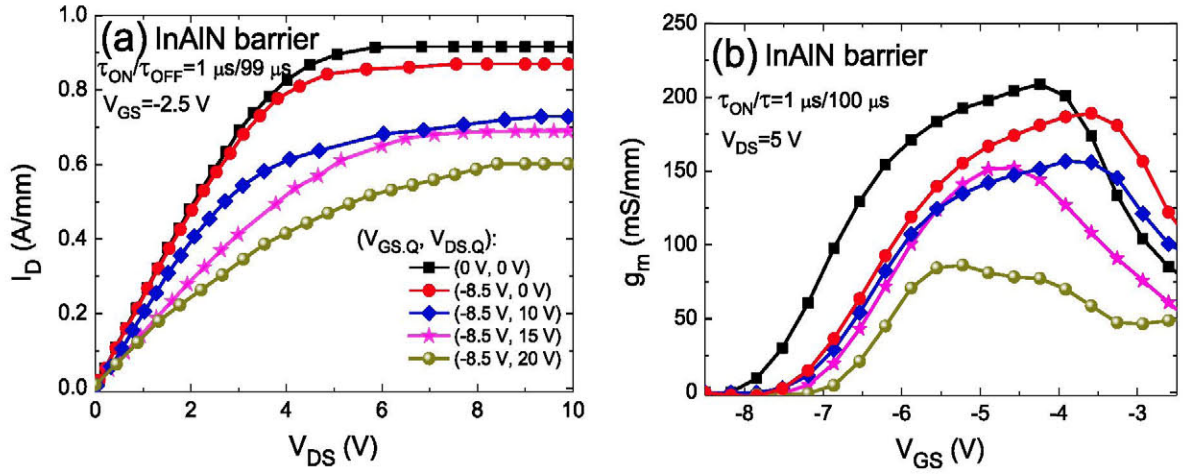

Figure 4. (a) I_D and (b) g_m (derived from I_D–V_{GS}) pulsed characterization for an InAlN barrier device.

quiescent bias point E (described in table 2). Besides the observed degradation of R_{ON}, they also showed a reduction of g_m (35% for the quiescent bias point E) without any V_{TH} shift, as shown in figure 3(b). Therefore, the current collapse in the AlGaN barrier devices was due to the presence of traps near the surface in the gate-drain access region [21, 25].

Concerning the InAlN barrier devices (figure 4), the B point is sufficient to induce a positive shift in the V_{TH} value, which indicates the presence of traps in the region under the gate [17]. Moreover, the increase of R_{ON} value as well as the reduction of the g_m (50% and 59% respectively, for E point) when V_{DS} quiescent voltage (C, D, and E points) revealed the trapping of electrons in the gate-to-drain region, which is activated by high gate-drain voltages (V_{GD}) [17, 20, 26].

Comparing the results obtained for AlGaN and InAlN barrier devices under test, we can deduce that the RF performance of InAlN HEMTs could be more dramatically affected by the presence of traps, even if they presented a better dc performance (see table 1).

I_D transient measurements were performed to study the capture and emission kinetics. They were carried out in the saturation region, as the signal related to capture and emission of electron is clearer than that obtained in the linear region.

Different filling trap voltages were used to evaluate which is the most adequate for the extraction of E_A. As figure 5(a) shows, an electron emission process (T1) and an electron capture process (T2) were detected for AlGaN barrier devices. The peak labeled as T1 was enhanced by filling pulses with very negative V_{GS}, which indicated that it was a gate-dependent trapping process. The chosen trap filling voltage was (−6 V, 8 V), since T1 related process had a typical time constant closer to the lower boundary of the acquisition window, which prevented the use of (−6, 20 V) to record this process at high temperatures. Figure 5(b) illustrates the differential signals related to the I_D transient measurements done in InAlN barrier devices. They revealed the presence of an electron emission process (T1′) and two electron capture processes (T2′, and T3′). The peak labeled as T1′ was detected when the filling voltage had very negative V_{GS}, which indicated that it was a gate-dependent trapping process; therefore, the chosen trap filling voltage was (−8.5 V, 8 V).

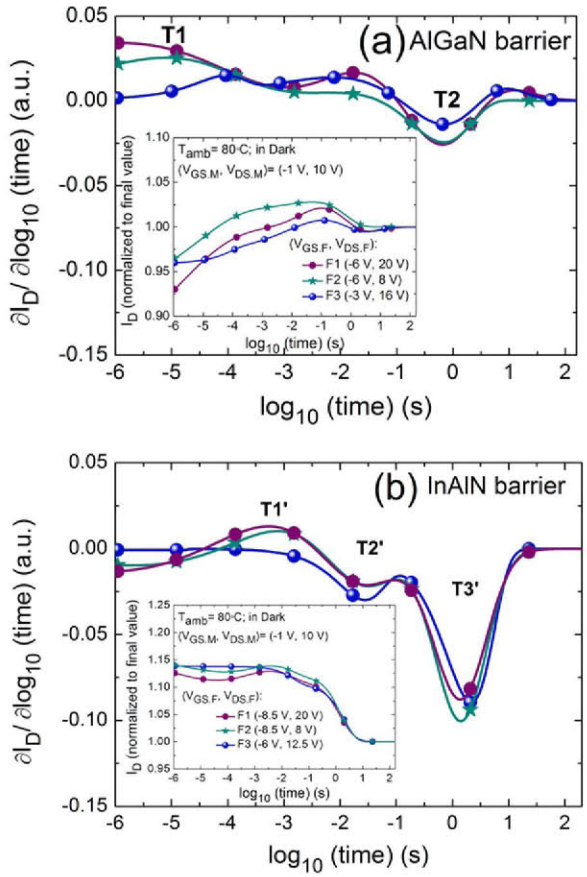

Figure 5. Differential signals for (a) AlGaN and (b) InAlN barrier devices which were extracted from the fitted I_D transient normalized to the final value shown in its corresponding inset figure.

Finally, I_D transient measurements at different T_{amb} from 40 °C to 120 °C were performed to extract the apparent E_A from the Arrhenius plot. Regarding AlGaN barrier devices, the value of E_A for T1 was 0.43 eV (±0.02 eV), as figure 6 shows. Interestingly, Arehart *et al* reported in [27] the

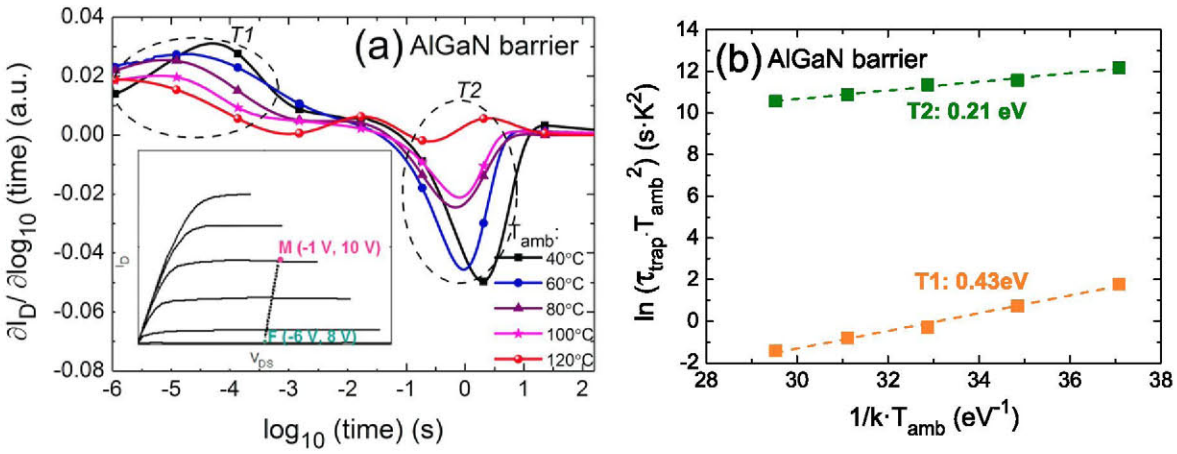

Figure 6. (a) Thermal activation and (b) Arrhenius plot with apparent activation energies for T1 and T2 in AlGaN barrier device.

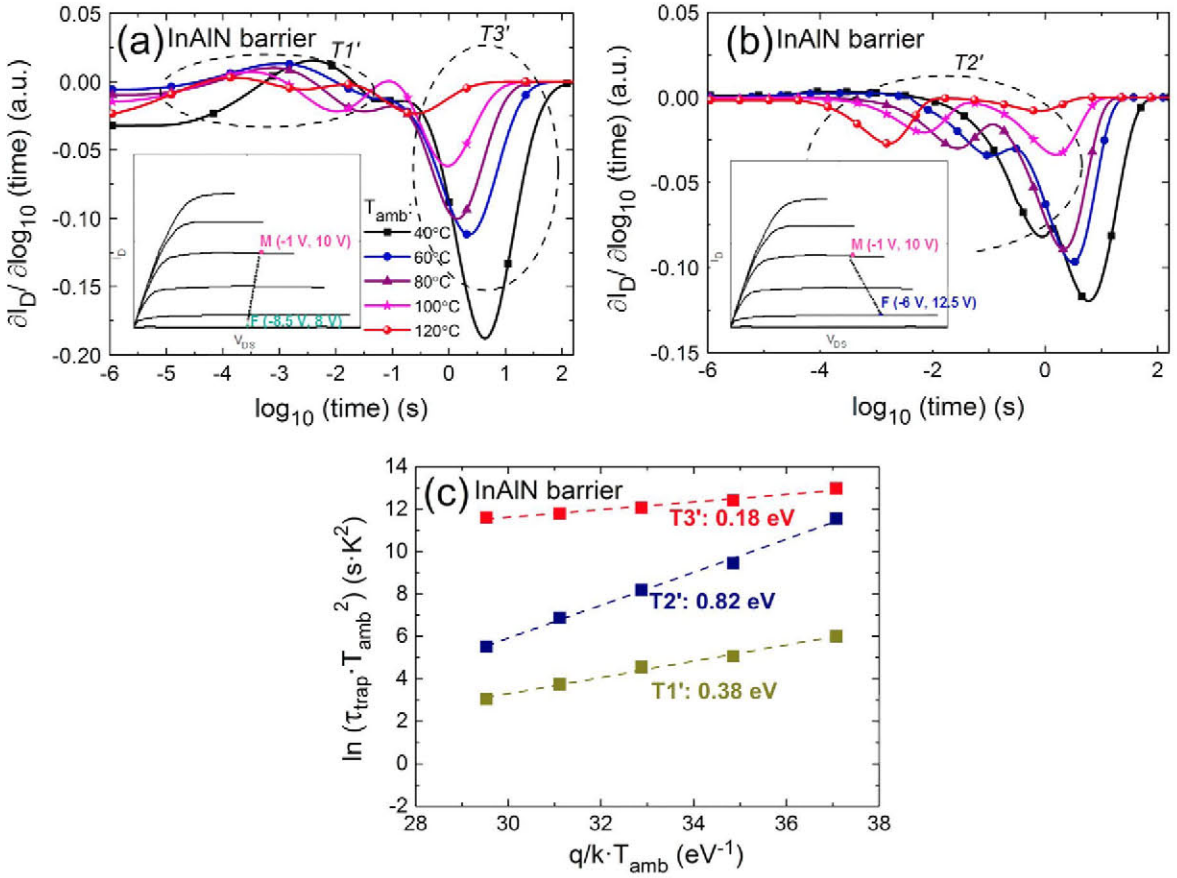

Figure 7. (a) Thermal activation corresponding to the trap filling voltage (−8.5 V, 8 V). (b) Thermal activation corresponding to the trap filling voltage (−6 V, 12.5 V). (c) Arrhenius plot with apparent activation energy corresponding to T1′, T2′ and T3′ for InAlN barrier device.

presence of traps in the access region with the same E_A level of 0.43 eV in AlGaN/GaN devices. They could be associated with C/O/H impurities [24, 28, 29]. For instance, Tapajna *et al* reported traps with similar E_A level (0.45 eV) in fresh devices located in the near-surface AlGaN region at the gate edge [24] which they attributed to the diffusion of impurities such as C and O into AlGaN close to the drain side of the gate. These impurities may be introduced during the growth of the structure.

On the other hand, the extracted E_A for T2 was 0.21 eV (±0.01 eV). Polyakov *et al* detected a hole trap with a very similar E_A of 0.20 eV [30]. They indicated that its possible location could be either the AlGaN barrier or the GaN buffer. Furthermore, Tirado *et al* reported the presence of donor type

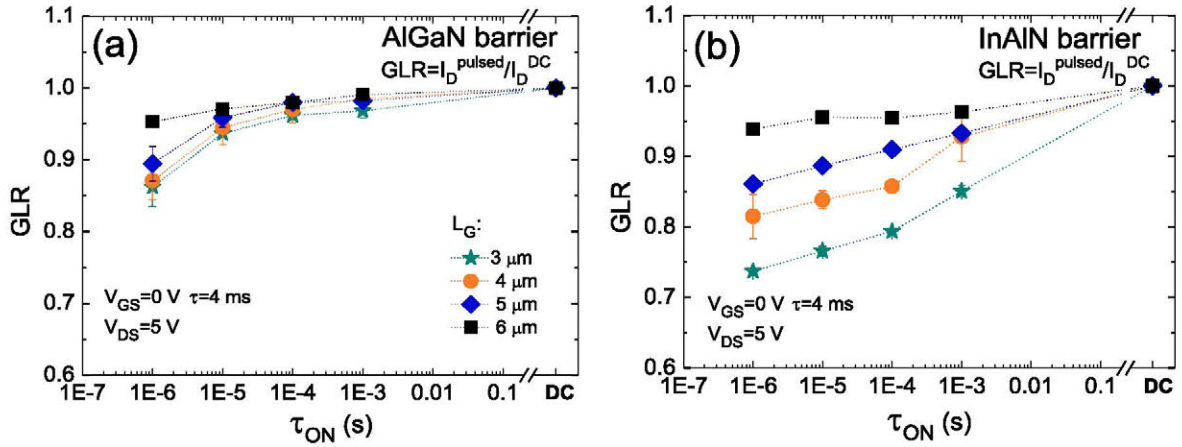

Figure 8. GLR calculated for (a) AlGaN and (b) InAlN barrier devices with fixed $L_{GD} = 15\ \mu$m and $W_G = 100\ \mu$m and varying L_G.

traps acting as hole traps with an E_A of 0.25 eV, uniformly distributed at the HEMT surface [16]. Although the origin of the donor surface traps is still a controversial issue, they are usually attributed to process damage, such as plasma and thermal damage, which generates nitrogen vacancies [31].

Regarding the InAlN barrier devices, the extracted E_A for T1′ was 0.38 eV (±0.02 eV), as shown in figure 7. A trap with similar E_A (0.37 eV) was previously detected in InAlN/GaN HEMTs by Chikhaoui *et al* [32]. They suggested that this trap state is located at the InAlN/metal interface, which could be in agreement with the positive shift in V_{TH} shown in figure 4(b). They associated this trap state to a structural defect, specifically to dislocations in the InAlN barrier layer.

On the other hand, the extracted E_A for the hole emission process T3′ was 0.18 eV (±0.01 eV). Whereas no reports regarding hole traps with this E_A value have been found in the literature for InAlN/GaN devices, Polyakov *et al* [30] determined hole traps with 0.18 eV for AlGaN/GaN HEMTs. Moreover, Faqir *et al* detected hole traps with identical E_A, which were assumed to be a donor surface trap [33]. This can be associated with state defects introduced during the device fabrication, similarly to the donor surface trap (0.21 eV) detected in AlGaN barrier devices.

Furthermore, I_D transient measurements using as filling trap voltage (−6 V, 12.5 V) were performed at varying T_{amb} (see figure 7(b)) in order to extract the E_A for the hole capture process. As figure 7(c) shows, it resulted in 0.82 eV (±0.01 eV). Although hole traps with this E_A have been not reported in InAlN/GaN devices yet, there is some literature related to these kinds of traps in AlGaN/GaN HEMTs. A donor-like trap with similar E_A to T2′ (0.86 eV) was reported by Polyakov *et al* for Fe-doped semi-insulating GaN structures [34]. Therefore, this trap could be introduced during the GaN buffer growth to achieve a semi-insulating behavior and hence is related to the material growth.

3.2. Impact of L_G and L_{GD} on trapping effects

Figure 5(a) reveals that the detected T1 and T2 in AlGaN barrier devices are gate-dependent processes. For InAlN barrier HEMTs, figure 5(b) shows that T1′ and T3′ are also gate-dependence processes. Therefore, V_{GS}-pulsed measurements were carried out in devices with different geometrical parameters to evaluate the impact of L_G and L_{GD} on trapping effects. The parameter chosen for the evaluation of the trapping effects was the gate lag ratio (GLR), which is defined as:

$$\mathrm{GLR} = \frac{I_{\mathrm{D.pulsed}}}{I_{\mathrm{D.DC}}} \tag{2}$$

where $I_{D.Pulsed}$ and $I_{D.DC}$ are the drain current measured under pulsed and dc biases, respectively.

Figure 8 illustrates the GLR as a function of τ_{ON} for AlGaN and InAlN barrier devices with $L_{GD} = 15\ \mu$m and $W_G = 100\ \mu$m and different L_G. These devices presented GLR values lower than 1 indicating the I_D collapse when V_{GS} changes abruptly, which can be explained by the 'virtual gate' effect [15]. This virtual gate is assumed to be located in the gate-drain region, being in series to the depletion layer underneath the gate [35] and it acts as a negatively biased gate due to the presence of negative charge on the surface [20, 36]. Whereas the gate electrode potential is controlled by the applied gate bias, the virtual gate potential is controlled by the total amount of trapped charge in the gate-drain access region. Therefore, the frequency dependence of I_D is linked to the time constants associated with charge de-trapping phenomena [36].

InAlN barrier devices presented more noticeable trapping effects than AlGaN barrier devices since they exhibited lower GLR values regardless of the device geometry (see figure 8). Furthermore, AlGaN and InAlN devices showed different time-dependence of I_D because the GLR value decreased dramatically for a different τ_{ON}, 1 μs and 1 ms in AlGaN and InAlN devices, respectively. Interestingly, devices with larger L_G led to higher GLR and hence, less current collapse. This confirms that lower trapping effects will be observed in devices with larger L_G and consequently, their dc-RF dispersion will be less noticeable.

Figure 9 shows the GLR as a function of τ_{ON} for AlGaN and InAlN barrier devices with $L_G = 3\ \mu$m, $W_G = 100\ \mu$m and different L_{GD}. It illustrates similar results to those previously shown in figure 8, which can be summarized as more trapping

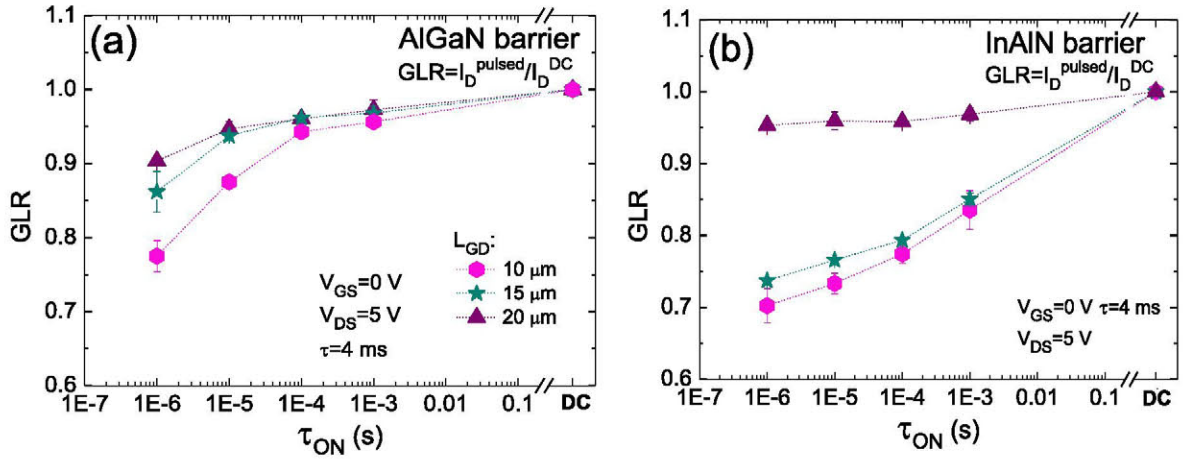

Figure 9. GLR calculated for (a) AlGaN and (b) InAlN barrier devices with fixed $L_G = 3\ \mu m$ and $W_G = 100\ \mu m$ and varying L_{GD}.

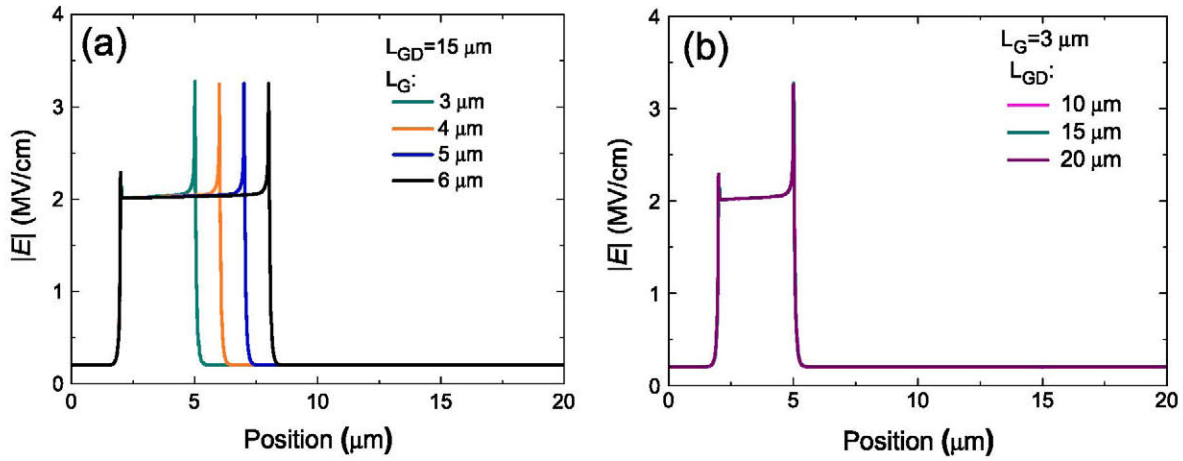

Figure 10. Distribution of electric field magnitude $|E|$ on the AlGaN surface as a function of (a) L_G from 3 μm to 6 μm and fixed $L_{GD} = 15\ \mu m$; (b) L_{GD} from 10 μm to 20 μm and fixed $L_G = 3\ \mu m$ (the curves in are overlapping). The position of maximum $|E|$ indicates the drain-side gate edge.

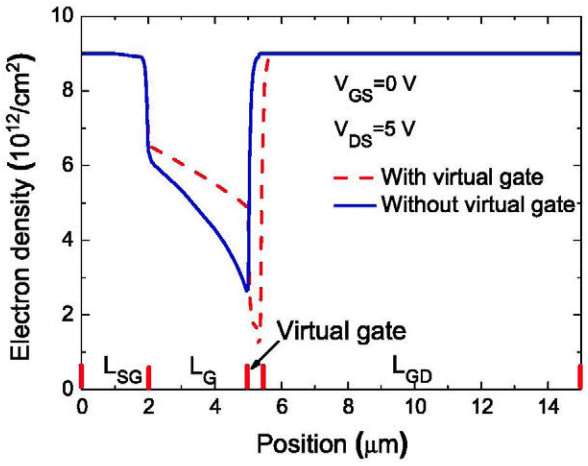

Figure 11. Comparison of electron density in the channel for the device with and without virtual gate. $L_{SG} = 2\ \mu m$, $L_G = 3\ \mu m$, $L_{GD} = 10\ \mu m$, and the virtual gate length indicated in the graph is 0.4 μm.

effects in InAlN barrier devices than in AlGaN barrier ones, and different time-dependence of I_D for AlGaN and InAlN barrier HEMTs. Moreover, devices with larger L_{GD} presented higher GLR and hence, less current collapse. This confirms that lower trapping effects, and hence lower dc-RF dispersion, will be observed in devices with larger L_{GD}.

In order to better understand the L_G and L_{GD} influences on the observed trapping effects, we performed the following simulations implemented using commercial software (COMSOL). Details of the simulation method can be found in [37]. The simulated device structure with AlGaN barrier was the same as that used in the experiments. We did not consider the detailed volume charge distribution since the GaN cap was very thin (1 nm), but considered it as surface charge on the AlGaN surface. According to the studies in [38], ionized donor-like traps (positively charged) were assumed on the AlGaN surface which can neutralize partial negative polarization charge. Note that the total surface charge density is a summation of positive charge of the ionized donor-like traps and the negative charge of the polarization. In the simulations, we fixed the polarization charge to 10^{13} q cm^{-2} at the AlGaN/

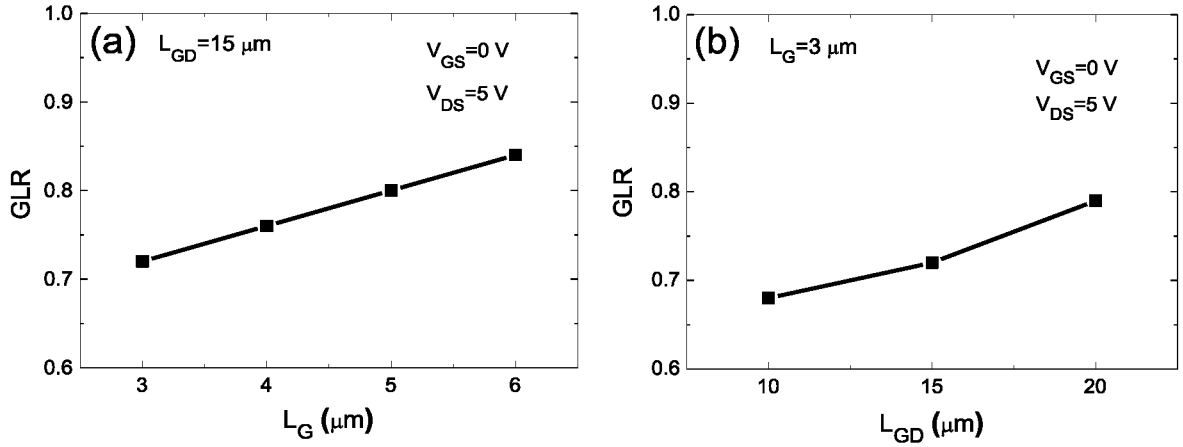

Figure 12. Simulated GLR as a function of L_G (a) and L_{GD} (b). The devices were biased in the knee region of the I_D ($V_{GS}=0$ V and $V_{DS}=5$ V, the same as the experimental biases).

Table 3. Summary of the results from the I_D transient measurements performed in the devices under test.

Device barrier	Process	Trap	E_A (eV)
AlGaN	Electron emission (T1)	Acceptor-like	0.43
	Hole emission (T2)	Donor-like	0.21
	Electron emission (T1′)	Acceptor-like	0.38
InAlN	Hole emission (T2′)	Donor-like	0.82
	Hole emission (T3′)	Donor-like	0.18

GaN interface and total charge of -1×10^{12} q cm^{-2} on the AlGaN surface to produce reasonable 2DEG density of 9×10^{12} cm^{-2} near the interface. When the device was biased in OFF-state, the donor-like traps near the drain-side gate edge were filled by the electrons tunneling from the gate metal. These filled traps were not charged and therefore led to higher density of the total negative surface charge and lower 2DEG density, usually termed 'virtual gate' phenomenon, as was previously explained.

Figure 10 shows the distribution of the simulated electric field magnitude |*E*| on the AlGaN surface as a function of L_G variation from 3 μm to 6 μm with fixed $L_{GD}=15$ μm, figure 10(a), and varying L_{GD} 10 μm to 20 μm with fixed $L_G=3$ μm, figure 10(b). The maximum |*E*| indicates the position of the drain-side gate edge. The devices were biased in OFF-state with $V_{GS}=-6$ V ($<V_{TH}$) and $V_{DS}=3.5$ V. In the simulations, a beveled gate edge was used in order to avoid the singularity of the electric field there, which was expected to be similar to the practical shape [39]. The maximum |E| and its distribution remained almost unchanged varying under L_G or L_{GD} variation. As we mentioned before, the surface traps were filled by the electrons tunneling from the gate metal. This tunneling current may be determined by |E|. The electron surface transport as well as transient process of trapping and de-trapping were not addressed as they go beyond the scope of the present work. It was unknown yet exactly about the electron transport mechanisms on the barrier surface, therefore we will neither address this nor the transient process of trapping and de-trapping in the simulations. However, due to the unchanged |*E*|, it is assumed that the devices with different geometries (different L_G or L_{GD}) have the same virtual gate length with the same probability of traps occupancy. Specifically, in the simulations, we set the virtual gate length as 0.4 μm with the total negative charge density of -9×10^{12} q cm^{-2}.

Figure 11 shows the simulated electron density for the device with and without virtual gate (see the indicated virtual gate in the graph). As expected, the electron density under the virtual gate was reduced significantly.

The simulated GLR as a function of L_G and L_{GD} are shown in figures 12(a) and (b), respectively. Note that we did not consider the pulse width that can determine the probability of traps occupancy. Therefore, $I_{D.Pulsed}$ and $I_{D.DC}$ were simulated for the device with (traps completely filled) and without (traps completely emptied) the virtual gate, respectively. GLR increased with increasing L_G or L_{GD}, showing a similar tendency compared to the experimental results displayed in figures 9 and 10.

The explanation for the simulation results is given in the following. For the device without virtual gate, $I_{D.DC}$ can be calculated as $I_{D.DC}=V_{DS}/R_T$, where R_T is the total resistance between the source and drain contact. For the device with virtual gate, $I_{D.Pulsed}$ can be calculated as $I_{D.Pulsed}=V_{DS}/(R_T+\Delta R_{VG})$, where ΔR_{VG} is the increased resistance caused by the virtual gate. Therefore, considering equation (2), GLR can be calculated as:

$$\mathrm{GLR} = I_{D.Pulsed}/I_{D.DC} = 1/\left[1+\left(\Delta R_{VG}/R_T\right)\right] \qquad (3)$$

ΔR_{VG} did not change for different device geometries due to the fixed virtual gate length and the fixed total charge density, as described before. Also, the devices were biased in the knee region of I_D ($V_{GS}=0$ V and $V_{DS}=5$ V, the same as the experimental biases), in which the access resistances between the gate and source/drain contact influenced by L_{SG} and L_{GD} are comparable to the channel resistance under the gate influenced by L_G. In other words, R_T does not mainly concentrate at the drain-side gate edge. Therefore, devices

with larger L_G or L_{GD} had larger R_T, smaller $\Delta R_{VG}/R_T$, and thus larger GLR.

4. Conclusion

We have evaluated the trap phenomena in AlGaN and InAlN barrier HEMTs. In spite of the better dc performance of InAlN barrier devices, they showed more remarkable trapping effects, in terms of higher I_D and g_m decrease and greater R_{ON} increase under double-pulsed conditions. The traps in the AlGaN barrier HEMTs under study were probably located in the gate-drain access region, since the double-pulsed characterization showed a decrease of g_m and I_D but without significant shift of V_{TH}. In contrast, our InAlN barrier devices presented a reduction of I_D associated with a positive V_{TH} shift, indicating the presence of traps under the gate region; as well as a degradation of both g_m and R_{ON} attributed to traps located in the gate-drain access region. I_D transient measurements enabled the identification of traps and the extraction of their E_A in devices with both AlGaN and InAlN barriers whose results are summarized in table 3. Finally, experiments and simulations confirmed the influence of device geometry on the observed trapping effects, which are less noticeable for devices with larger L_G or L_{GD}.

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